

CA-IS309x 5kV_{RMS} Isolated RS-485 Transceivers with Integrated DC-DC Converter

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
 - Data rate: up to 20Mbps for CA-IS3098 and 0.5Mbps for CA-IS3092
 - 1/8 unit load enables up to 256 nodes on the bus
 - 3V to 5.5V supply voltage range, and the CA-IS3092VW/CA-IS3098VW provide individual logic supply input
- **Integrated DC-DC Converter for Cable-side Power**
 - 3.3V and 5V output options ($V_{ISO} \leq V_{CC}$)
 - High integration with internal transformer
 - Soft-start reduces input inrush current
 - Overload and short-circuit protection
 - Thermal shutdown
- **Integrated Protection for Robust Communication**
 - 5kV_{RMS} withstand isolation voltage for 60s (galvanic isolation)
 - $\pm 150\text{kV}/\mu\text{s}$ typical CMTI
 - High lifetime: >40 years
 - $\pm 20\text{kV}$ Human Body Model(HBM) ESD protection on bus I/O, $\pm 6\text{kV}$ HBM ESD protection on logic I/O
 - True fail-safe guarantees known receiver output state
 - Wide operating temperature range: -40°C to 125°C
- **Wide-body SOIC16-WB(W) Package**
- **Safety Regulatory Approvals**
 - $7070V_{PK} V_{IOTM}$ and $1414V_{PK} V_{IORM}$ per DIN VDE V0884-17:2021-10
 - 5kV_{RMS} isolation for 1 minute per UL 1577
 - IEC 60950-1, IEC 60601-1 and EN 61010-1 certifications
 - CQC, TUV, and CSA certifications

2. Applications

- Industrial Automation Equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

3. General Description

The CA-IS309x family of devices is galvanically-isolated RS-485 transceivers with built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO₂) insulation barrier that provides up to 5kV_{RMS} (60s) of galvanic isolation and $\pm 150\text{kV}/\mu\text{s}$ typical CMTI. Isolation improves data communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports. An integrated DC-DC converter generates the 3.3V or 5V operating voltage for the cable-side.

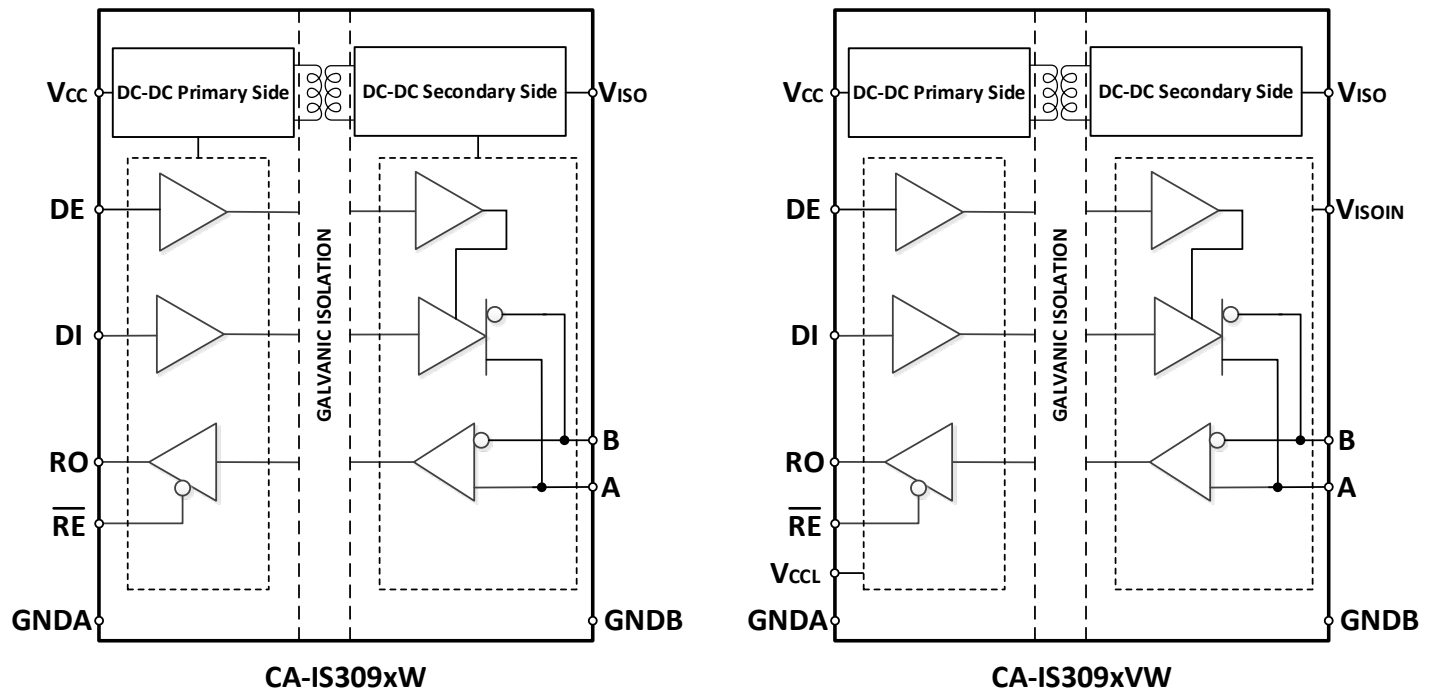
The CA-IS309x family of devices is designed for high-speed multi-drop operation with high ESD protection of up to $\pm 20\text{kV}$ HBM on the bus pins. The receiver is 1/8-unit load, allowing up to 256 transceivers (loads) on a common bus. The CA-IS3092W/CA-IS3092VW and CA-IS3098W/CA-IS3098VW provide half-duplex transceivers, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements. The individual logic supply input of CA-IS3092VW and CA-IS3098VW devices allows fully compatible 2.7V to 5.5V logic on logic input/output lines.

The CA-IS309x series devices are available in wide-body 16-pin SOIC package which are the industry standard isolated RS-485 package, and operate over -40°C to $+125^{\circ}\text{C}$ temperature range.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3092W CA-IS3092VW CA-IS3098W CA-IS3098VW	SOIC16-WB(W)	10.30 mm × 7.50 mm

CA-IS309x Function Diagram



4. Ordering Information

Table 4-1. Ordering Information

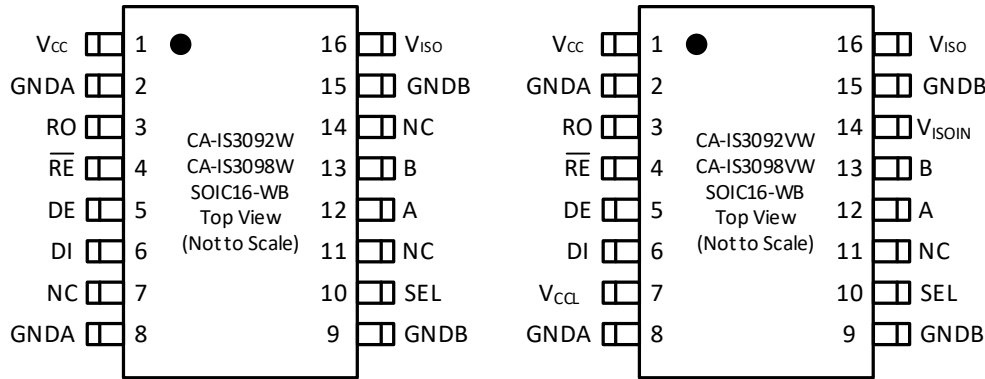
Part Number	Full/half duplex	Data Rate (Mbps)	V _{ISO} (V)	V _{DDL}	Package
CA-IS3092W	Half-Duplex	0.5	3.3/5.0	No	SOIC16-WB(W)
CA-IS3092VW	Half-Duplex	0.5	3.3/5.0	Yes	SOIC16-WB(W)
CA-IS3098W	Half-Duplex	20	3.3/5.0	No	SOIC16-WB(W)
CA-IS3098VW	Half-Duplex	20	3.3/5.0	Yes	SOIC16-WB(W)

Contents

1. Features	1	8. Parameter Measurement Information	15
2. Applications	1	9. Detailed Description	18
3. General Description	1	9.1. Logic Input	18
4. Ordering Information	2	9.2. Fail-Safe Receiver	18
5. Revision History	3	9.3. Driver	19
6. Pin Configuration and Description	4	9.4. Protection Functions.....	19
7. Specifications	5	9.4.1. Signal Isolation and Power Isolation	19
7.1. Absolute Maximum Ratings ¹	5	9.4.2. Undervoltage Lockout	19
7.2. ESD Ratings.....	5	9.4.3. Thermal Shutdown.....	20
7.3. Recommended Operating Conditions	5	9.4.4. Current-Limit	20
7.4. Thermal Information	5	9.5. Isolated Supply Output	20
7.5. Insulation Specifications.....	6	10. Applications Information	21
7.6. Safety-Related Certifications (pending).....	7	10.1. Overview	21
7.7. Electrical Characteristics	8	10.2. Typical Application	22
7.7.1. Driver.....	8	10.3. 256 transceivers on the bus.....	22
7.7.2. Receiver.....	8	10.4. PCB Layout	22
7.8. Supply Current	9	11. Package Information	24
7.9. Switching Characteristics.....	10	12. Soldering Temperature (reflow) Profile	25
7.9.1. Driver.....	10	13. Tape And Reel Information	26
7.9.2. Receiver.....	10	14. Important Statement	27
7.10. Typical Operating Characteristics	11		

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.02	Changed bypass capacitor value.	21
Version 1.03	Added PCB layout description.	22
Version 1.04	Created individual CA-IS3092/CA-IS3098 datasheet. Added new parts of CA-IS3092VW and CA-IS3098VW. Updated Typical Operating Characteristics.	All 2, 25 10
Version 1.05	Updated PCB layout Guidelines. Added data rate x load capacitance limitation.	3 19
Version 1.06	Updated POD	26
Version 1.07	Updated UL certification information	7
Version 1.08	Figure10-1 Cable Side GNDA changed to GNDB	20
Version 1.09	Change driver enable time and driver disable time Change receiver propagation delay Parameter Measurement Information	9 9 14
Version 1.10	Update VDE,TUV information	6,7

6. Pin Configuration and Description

Figure 6-1. CA-IS3092W/CA-IS3098W/CA-IS3092VW/CA-IS3098VW SOIC16 Top View
Table 6-1. CA-IS3092W/CA-IS3098W/CA-IS3092VW/CA-IS3098VW Pin Description and Functions

Name	PIN Number		Type	Description
	CA-IS3092W CA-IS3098W	CA-IS3092VW CA-IS3098VW		
V _{CC}	1	1	Power Supply	Logic-Side Power Input and DC-DC converter supply input. Bypass V _{CC} to GNDA with both 0.1μF and at least 10μF capacitors as close to the device as possible.
GNDA	2, 8	2, 8	GND	Logic-Side Ground. GNDA is the ground reference for digital signals of logic side.
RO	3	3	Digital I/O	Receiver Data Output. Drive \overline{RE} low to enable receiver R _x . With \overline{RE} low, RO is high when (V _A - V _B) > -20mV and is low when (V _A - V _B) < -200mV. RO is high impedance when \overline{RE} is high.
\overline{RE}	4	4	Digital I/O	Receiver Output Enable. Driver \overline{RE} low or connect to GNDA to enable R _x . Drive \overline{RE} high to disable R _x . RO is high-impedance when \overline{RE} is high.
DE	5	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
V _{CC1} ¹	---	7	Power Supply	Logic-supply input. V _{CC1} is the logic supply voltage for logic-side input/output. Bypass to GNDA with a 1μF capacitor.
GNDB	9, 15	9, 15	GND	Cable Side Ground. GNDB is the ground reference for the RS-485 bus signals.
SEL ²	10	10	Digital I/O	Output voltage V _{ISO} select pin: V _{ISO} = 5.0 V when SEL is shorted to V _{ISO} ; V _{ISO} = 3.3 V when SEL is shorted to GNDB or floating;
NC	7, 11, 14	11	---	No internal connection
A	12	12	Bus I/O	Non-inverting RS-485 receiver input and driver output.
B	13	13	Bus I/O	Inverting RS-485 receiver input and driver output.
V _{ISOIN}	---	14	Power Supply	Cable side power supply input. Bypass V _{ISOIN} to GNDB with at least 1μF capacitor as close to the device as possible.
V _{ISO}	16	16	Power Supply	Isolated DC-DC power supply output. Cable Side Power supply. Bypass V _{ISO} to GNDB with both 0.1μF and at least 10μF capacitors as close to the device as possible.

Notes:

- Logic-Supply Input. V_{CC1} can be different voltage from V_{CC} supply, which allows fully compatible +2.7V to +5.5V logic for digital input/output.
- V_{ISO} ≤ V_{CC}, this means if V_{CC} = 3.3V, SEL pin must be floating or connected to GNDB and set the V_{IOs} output to 3.3V; if V_{CC} = 5.0V, there is no connection limit for SEL pin.

7. Specifications

7.1. Absolute Maximum Ratings¹

PARAMETER	MIN	MAX	UNIT
V_{CC}, V_{CCL}	-0.5	6.0	V
V_{ISO}, V_{ISOIN}	-0.5	6.0	V
V_{IO1}	-0.5	$V_{CC}/V_{CCL} + 0.5^3$	V
V_{IO2}	-0.5	$V_{ISO}/V_{ISOIN} + 0.5^3$	V
V_{BUS}	-8	13	V
I_O	-20	20	mA
T_J		150	°C
T_{STG}	-65	150	°C

Notes:

- The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 6V.

7.2. ESD Ratings

PARAMETER	VALUE	UNIT
V_{ESD} Electrostatic discharge	Bus pins to GNDB	±20
	Other pins on cable-side to GNDB	±6
	All pins on logic-side to GNDA	±6
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ²	±2	kV

Notes:

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

PARAMETER	Min	Typ.	Max	Unit
V_{CC}^1	3.15	3.3 or 5	5.5	V
V_{CCL}	2.375	3.3 or 5	5.5	V
V_{OC}	-7		12	V
V_{ID}	-12		12	V
RL	54			Ω
V_{IH}	2.0		$V_{CC}/V_{CCL} + 0.3$	V
V_{IL}	-0.3		0.8	V
V_{IH}	$0.7 \times V_{CC}/V_{CCL}$		$V_{CC}/V_{CCL} + 0.3$	V
V_{IL}	-0.3		$0.3 \times V_{CC}/V_{CCL}$	V
DR			0.5	Mbps
DR			10	Mbps
T_A	-40		125	°C

Note:

- $V_{ISO} \leq V_{CC}$, this means if $V_{CC} = 3.3V$, SEL pin must be floating or connected to GNDB and set the V_{IOs} output to 3.3V; if $V_{CC} = 5.0V$, there is no connection limit for SEL pin.

7.4. Thermal Information

THERMAL METRIC	CA-IS309x	Unit
	SOIC16-WB(W)	
$R_{\theta JA}$	68.5	°C/W

7.5. Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			W	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN V VDE V 0884-17:2021-10¹				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	V _{RMS}
		DC voltage	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t=60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t=1 s (100% product test)	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ²	Test method per IEC 60065, 1.2/50μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	V _{PK}
Q _{pd}	Apparent charge ³	Method a, after input/output safety tests subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s	≤5	
C _{IO}	Barrier capacitance, input to output ⁴	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance, input to output ⁴	V _{IO} = 500V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum isolation voltage	V _{TEST} = V _{ISO} , t = 60s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1s (100% production)	5000	V _{RMS}
Notes:				
1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.				
2. Devices are immersed in oil during surge characterization.				
3. The characterization charge is discharging charge (pd) caused by partial discharge.				
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

7.6. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN V VDE V 0884-17:2021-10	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Maximum transient isolation voltage: 7070V _{pk} Maximum repetitive peak isolation voltage: 1414V _{pk} Maximum surge isolation voltage: 8000V _{pk}	Maximum isolation voltage: 5000 V _{RMS}	Maximum isolation voltage: 5000 V _{RMS}	Isolation rating: 5000Vrms
Certificate number: 40057278 (reinforced isolation)	Certification number: E511334	Certification number: CQC23001406424	Certification number: CN23RC4J 001

7.7. Electrical Characteristics
7.7.1. Driver

All typical specs are at $V_{CC} = 5V$, $V_{CCL} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter	Test Condition	Min	Typ.	Max	Unit
V _{OD1}	Driver differential output voltage I _O = 0mA, unloaded bus. SEL = LOW or float		2.9		V
		I _O = 0mA, unloaded bus. SEL = HIGH	3.7	4.6	
V _{OD2}	Driver differential output voltage R _L =54Ω, see Figure 8-1, SEL = LOW or float		1.5	2	V
		R _L =54Ω, see Figure 8-1, SEL = HIGH	2.1	3.6	
V _{OD3}	Driver differential output voltage with bus load V _{test} = -7V to 12V, see Figure 8-1	1.5			V
Δ V _{OD1}	Change in differential output voltage between two states R _L =54Ω, or R _L =100Ω, see Figure 8-1	-0.2		0.2	V
V _{OC}	Common-mode output voltage R _L =54Ω, or R _L =100Ω, see Figure 8-1	1	V _{ISO} /2	3	V
ΔV _{OC}	Change in steady-state common-mode output voltage between two states R _L =54Ω, or R _L =100Ω, see Figure 8-1	-0.2		0.2	V
I _{IH} , I _{IL}	Input leakage current DI, DE = low or high	-20		20	μA
I _{os}	Short-circuit output current (V _O = HIGH) DE = V _{CC} , DI = 0V or V _{CC} , V _A or V _B = -7V	-150		150	mA
		DE = V _{CC} , DI = 0V or V _{CC} , V _A or V _B = 12V			
CMTI	Common mode transient immunity V _{CM} = 1200V; See Figure 8-6	100	150		kV/ μS

7.7.2. Receiver

All typical specs are at $V_{CC} = 5V$, $V_{CCL} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter	Test Condition	Min	Typ.	Max	Unit
V _{OH}	V _{CC} =5V, I _{OH} =4mA	V _{CC} -0.4	4.8		V
	V _{CC} =3.3V, I _{OH} =-4mA	V _{CC} -0.4	3		
V _{OL}	V _{CC} =5V, I _{OL} =4mA		0.2	0.4	V
	V _{CC} =3.3V, I _{OL} =4mA		0.2	0.4	
V _{IT+(IN)}	Positive-going input threshold voltage		-110	-50	mV
V _{IT-(IN)}	Negative-going input threshold voltage	-200	-140		mV
V _{I(HYS)}	Receiver input hysteresis		30		mV
I _I	V _A or V _B = 12V, other inputs = 0 V		75	125	μA
	V _A or V _B = 12V, V _{CC} = 0 V, other inputs = 0 V		80	125	
	V _A or V _B = -7 V, other inputs = 0 V	-100	-40		
	V _A or V _B = -7 V, V _{CC} = 0 V, other inputs = 0 V	-100	-40		
I _{IH}	Input current on \overline{RE} pin V _{IH} = V _{CC}	-20		20	μA
I _{IL}	Input current on \overline{RE} pin V _{IL} = 0 V	-20		20	μA
R _{ID}	Differential input resistance A, B, -7V < V _{CM} < 12V	96			KΩ

7.8. Supply Current

 All typical specs are at $V_{CC} = 5V$, $V_{CCL} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions.

Parameter		Test Condition	Min	Typ.	Max	Unit
Isolated Power Supply (without bus load across A and B, unless otherwise specified.)						
V_{ISO}	Isolated supply output	$I_{ISO} = 0$ to 130mA, $V_{CC} = 5V$, SEL = GNDB or V_{ISO}	4.75	5	5.25	V
		$I_{ISO} = 0$ to 75mA, $V_{CC} = 3.3V$, SEL = GNDB	3.13	3.3	3.47	
I_{ISO}	Maximum load current ¹	$R_L = NC^2$	$V_{CC} = 5V$, SEL = GNDB or V_{ISO}	130		mA
			$V_{CC} = 3.3V$, SEL = GNDB	75		
		$R_L = 100\Omega$	$V_{CC} = 5V$, SEL = V_{ISO}	80		
			$V_{CC} = 5V$, SEL = GNDB	105		
			$V_{CC} = 3.3V$, SEL = GNDB	40		
		$R_L = 54\Omega$	$V_{CC} = 5V$, SEL = V_{ISO}	55		
			$V_{CC} = 5V$, SEL = GNDB	85		
			$V_{CC} = 3.3V$, SEL = GNDB	30		
$V_{ISO(LINE)}$	DC line regulation	$I_{ISO} = 50mA$, $V_{CC} = 4.5$ to 5.5V, SEL = GNDB or V_{ISO}	2		mV/V	
		$I_{ISO} = 50mA$, $V_{CC} = 3.15$ to 3.6V, SEL = GNDB				
$V_{ISO(LOAD)}$	DC load regulation	$I_{ISO} = 0$ to 130mA, $V_{CC} = 5V$, SEL = GNDB or V_{ISO}	1%			
		$I_{ISO} = 0$ to 75mA, $V_{CC} = 3.3V$, SEL = GNDB				
EFF	Efficiency @ maximum load current	$I_{ISO} = 130mA$, $C_{LOAD} = 0.1\mu F // 10\mu F$	$V_{CC} = 5V$, SEL = V_{ISO}	53%		
			$V_{CC} = 5V$, SEL = GNDB	42%		
		$I_{ISO} = 75mA$, $C_{LOAD} = 0.1\mu F // 10\mu F$	$V_{CC} = 3.3V$, SEL = GNDB	47%		
Quiescent current, $DE = V_{CC}$, $\overline{RE} = 0V$, $DI = 0V$						
I_{CC}	Supply current on logic side	$R_L = NC^2$	$V_{CC} = 3.3V$, SEL = GNDB	17	28	mA
			$V_{CC} = 5.0V$, SEL = GNDB	15	22	
			$V_{CC} = 5.0V$, SEL = V_{ISO}	18	28	
		$R_L = 54\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	94	125	
			$V_{CC} = 5.0V$, SEL = GNDB	82	120	
			$V_{CC} = 5.0V$, SEL = V_{ISO}	140	200	
		$R_L = 100\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	65	95	
			$V_{CC} = 5.0V$, SEL = GNDB	55	80	
			$V_{CC} = 5.0V$, SEL = V_{ISO}	93	135	
		$R_L = 120\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	57	88	
			$V_{CC} = 5.0V$, SEL = GNDB	50	72	
			$V_{CC} = 5.0V$, SEL = V_{ISO}	83	120	
CA-IS3092 Operating current, $DE = V_{CC}$, $\overline{RE} = 0V$, $DI = 250kHz$ square-wave, 50% duty cycle.						
I_{CC}	Supply current on logic side	$R_L = 54\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	92	125	mA
			$V_{CC} = 5V$, SEL = GNDB	85	120	
			$V_{CC} = 5V$, SEL = V_{ISO}	145	210	
		$R_L = 100\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	65	95	
			$V_{CC} = 5V$, SEL = GNDB	60	85	
			$V_{CC} = 5V$, SEL = V_{ISO}	100	145	
		$R_L = 120\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	60	85	
			$V_{CC} = 5V$, SEL = GNDB	55	80	
			$V_{CC} = 5V$, SEL = V_{ISO}	95	140	
CA-IS3098 Operating current, $DE = V_{CC}$, $\overline{RE} = 0V$, $DI = 10MHz$ square-wave, 50% duty cycle.						
I_{CC}	Supply current on logic side	$R_L = 54\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	68	107	mA
			$V_{CC} = 5V$, SEL = GNDB	66	96	
			$V_{CC} = 5V$, SEL = V_{ISO}	121	182	
		$R_L = 100\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	55	87	
			$V_{CC} = 5V$, SEL = GNDB	47	67	
			$V_{CC} = 5V$, SEL = V_{ISO}	83	126	
		$R_L = 120\Omega$	$V_{CC} = 3.3V$, SEL = GNDB	50	79	
			$V_{CC} = 5V$, SEL = GNDB	38	55	
			$V_{CC} = 5V$, SEL = V_{ISO}	69	106	

Notes:

1. $DE = V_{CC}$, $\overline{RE} = 0V$, $DI = 0V$ or V_{CC} ; The available output current from V_{ISO} will be reduced when $T_A > 85^\circ C$, see Figure 7-14, Figure 7-16, Figure 7-18, the maximum output current of V_{ISO} vs. temperature.
2. R_L is bus load across A and B, $R_L = NC$ means no-load connection between CANH and CANL.

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at $V_{CC} = 5V$, $V_{CCL} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters	Test conditions	Minimum value	TYP	Maximum value	Unit
CA-IS3092					
t_{PLH}, t_{PHL}	Driver Propagation Delay		100	250	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-2	5	20	ns
t_r, t_f	Differential output rise/full time		150	500	ns
t_{PZH}, t_{PZL}	Driver enable time		300	800	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 8-3	20	50	ns
CA-IS3098					
t_{PLH}, t_{PHL}	Driver Propagation Delay		20	50	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-2	3	12.5	ns
t_r, t_f	Differential output rise/full time		5	12	ns
t_{PZH}, t_{PZL}	Driver enable time		300	800	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 8-3	15	35	ns

7.9.2. Receiver

All typical specs are at $V_{CC} = 5V$, $V_{CCL} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters	Test conditions	Minimum value	TYP	Maximum value	Unit
CA-IS3092					
t_{PLH}, t_{PHL}	Receiver propagation delay		50	100	ns
t_{PWD}	Receiver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-4.		12	ns
t_r, t_f	Receiver output rise/full time		2.5	4	ns
t_{PHZ}, t_{PLZ}	Receiver disable time		20	50	ns
t_{PZH}, t_{PZL}	Receiver enable time, $DE = 0V$	See Figure 8-5.	30	80	ns
CA-IS3098					
t_{PLH}, t_{PHL}	Receiver propagation delay		40	80	ns
t_{PWD}	Receiver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-4.		8	ns
t_r, t_f	Receiver output rise/full time		2.5	4	ns
t_{PHZ}, t_{PLZ}	Receiver disable time		20	50	ns
t_{PZH}, t_{PZL}	Receiver enable time, $DE = 0V$	See Figure 8-5.	30	80	ns

7.10. Typical Operating Characteristics

All typical specs are at $V_{CC} = 5V$, $V_{CC_L} = V_{CC}$, $V_{ISOIN} = V_{ISO}$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

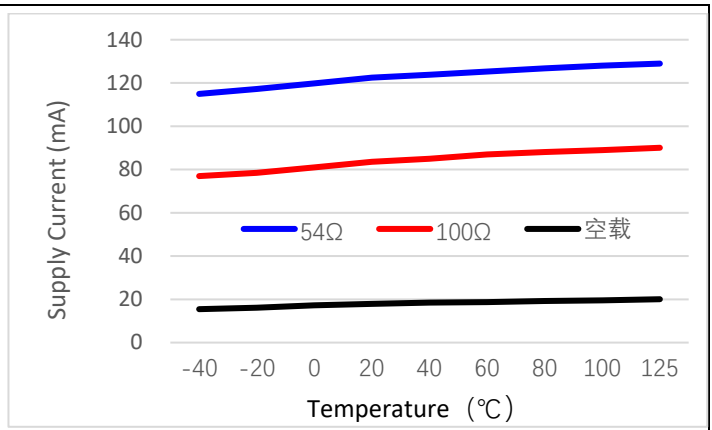
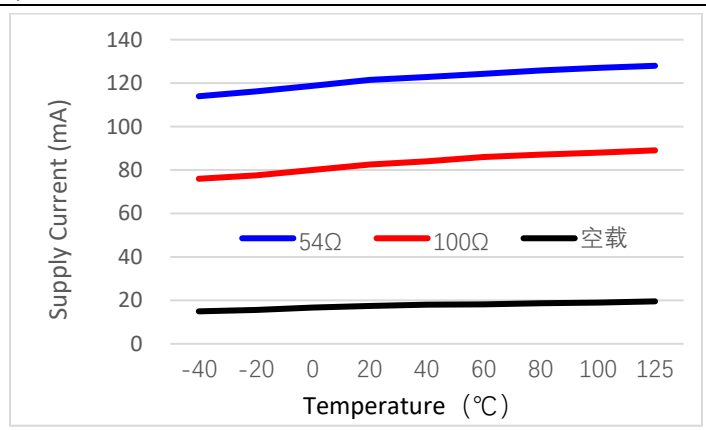


Figure 7-1.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3092x, $V_{CC} = 5V$, $V_{ISO} = 5V$, DR = 500kbps

Figure 7-2.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3098x, $V_{CC} = 5V$, $V_{ISO} = 5V$, DR = 20Mbps

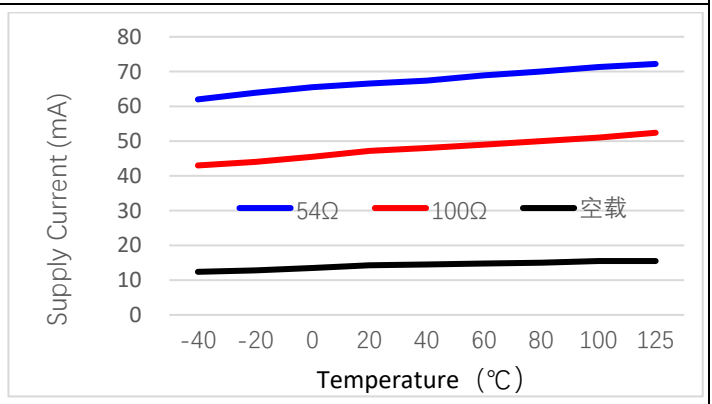
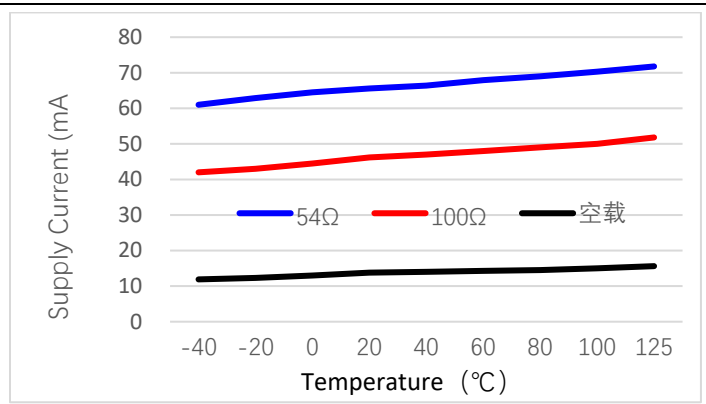


Figure 7-3.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3092x, $V_{CC} = 5V$, $V_{ISO} = 3.3V$, DR = 500kbps

Figure 7-4.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3098x, $V_{CC} = 5V$, $V_{ISO} = 3.3V$, DR = 20Mbps

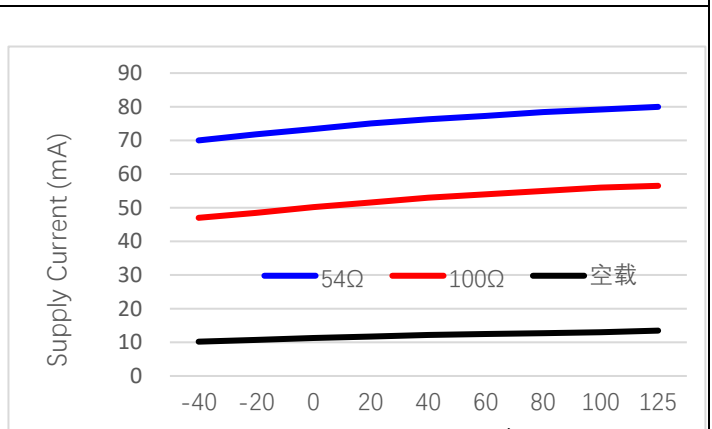
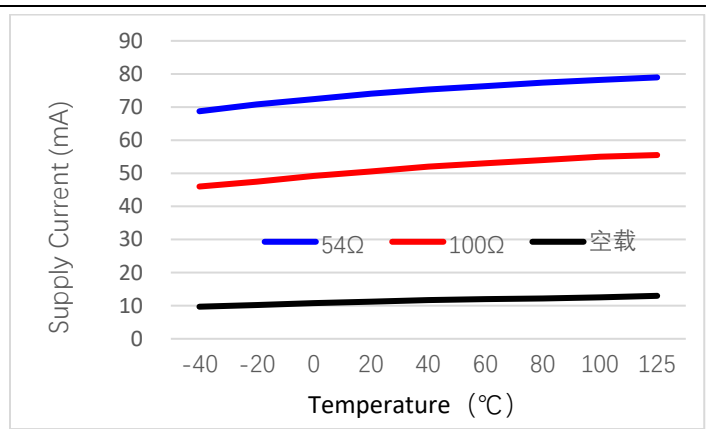


Figure 7-5.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3092x, $V_{CC} = 3.3V$, $V_{ISO} = 3.3V$, DR = 500kbps

Figure 7-6.
Logic-side supply current (I_{CC}) at different bus load
CA-IS3098x, $V_{CC} = 3.3V$, $V_{ISO} = 3.3V$, DR = 20Mbps

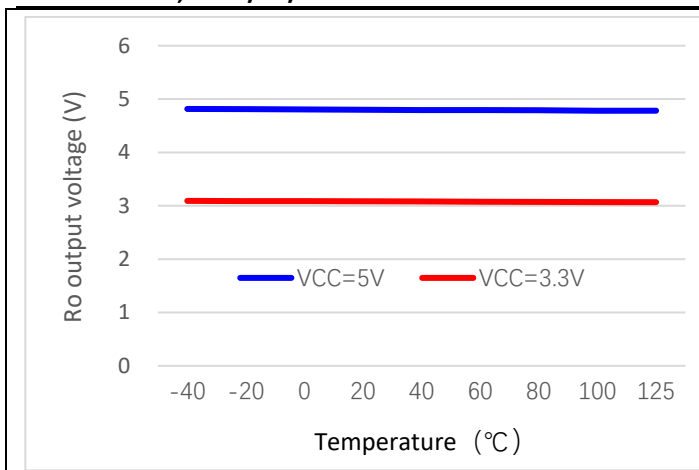


Figure 7-7.
Ro = High, Ro pull-down current = 4mA

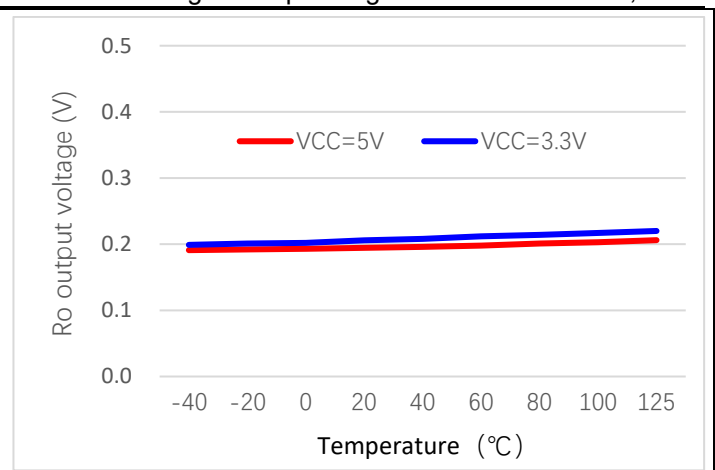


Figure 7-8.
Ro = Low, Ro pull-up current = 4mA

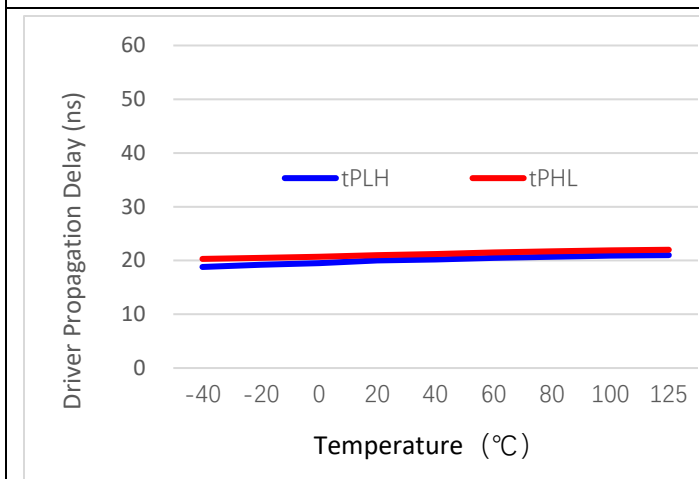


Figure 7-9.
CA-IS3092x driver propagation delay
V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = 54Ω

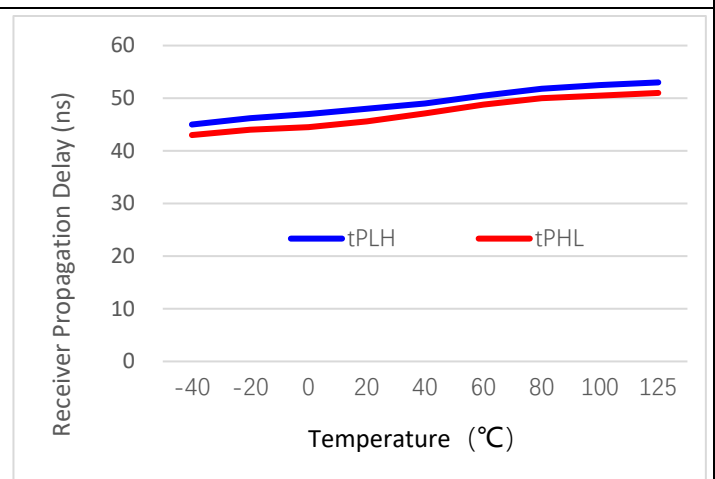


Figure 7-10.
CA-IS3092x receiver propagation delay
V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = 54Ω

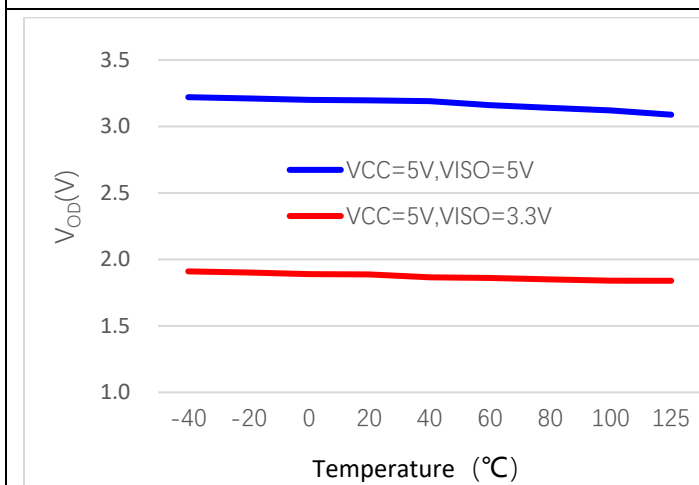


Figure 7-11.
Differential output voltage V_{OD}, R_L = 54Ω, V_{CC} = 5V

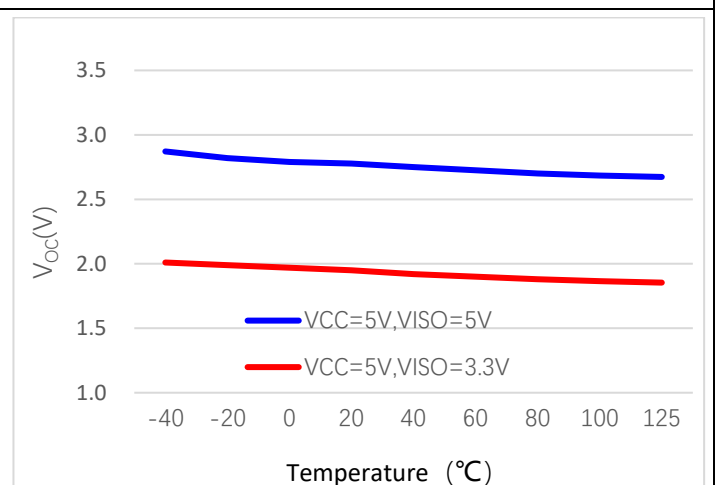


Figure 7-12.
Common-mode output voltage V_{OC}, R_L = 54Ω, V_{CC} = 5V

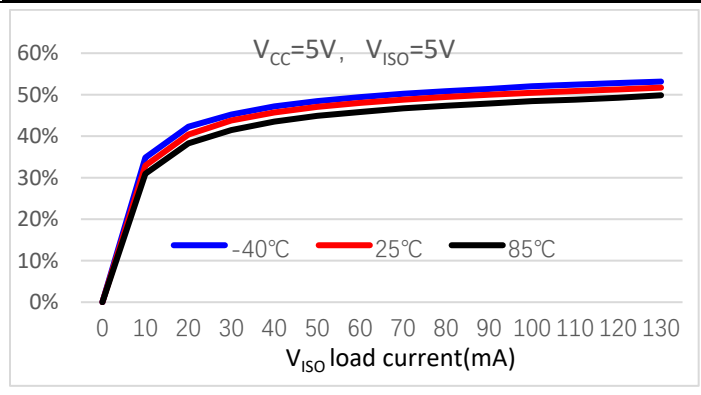


Figure 7-13.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
 $V_{CC} = 5V, V_{ISO} = 5V, R_L = NC$

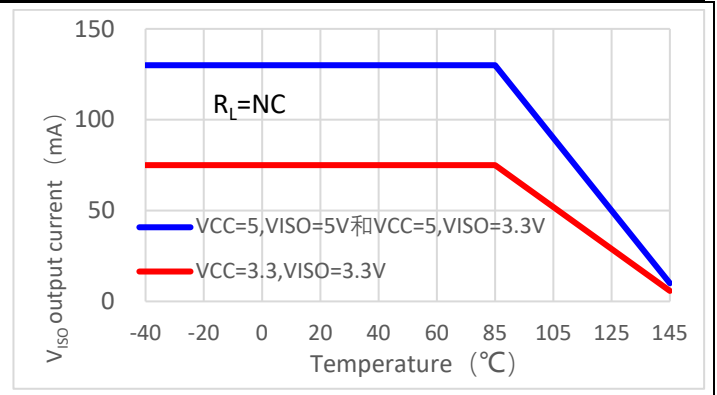


Figure 7-14.
Maximum output current from V_{ISO} vs. temperature with $R_L = NC$
Without data transmission (CA-IS309x)

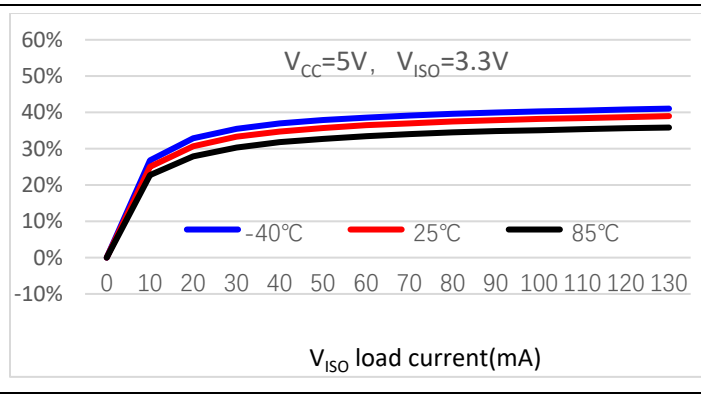


Figure 7-15.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
 $V_{CC} = 5V, V_{ISO} = 3.3V, R_L = NC$

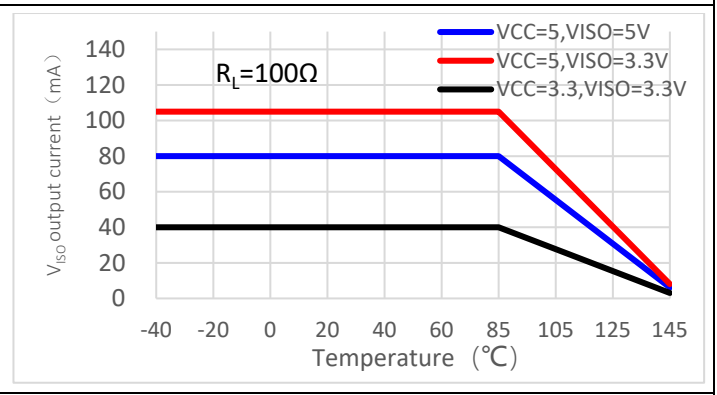


Figure 7-16.
Maximum output current from V_{ISO} vs. temperature with $R_L = 100\Omega$
CA-IS3092x: DR = 500kbps, $C_L = 2nF$
CA-IS3098x: DR = 20Mbps, $C_L = 200pF$

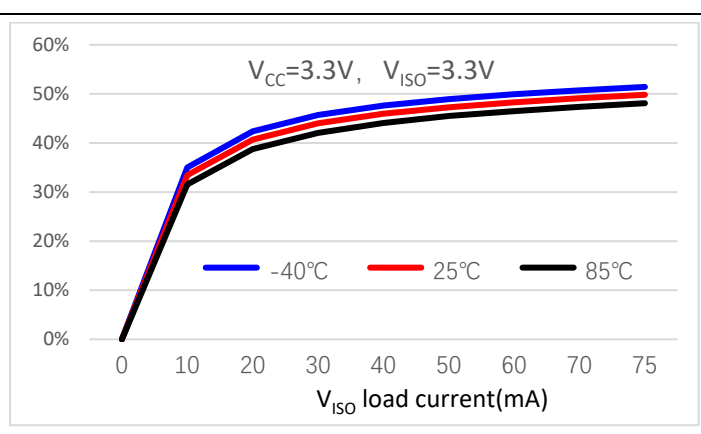


Figure 7-17.
Efficiency vs. load current (I_{ISO}) at different ambient temperature
 $V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = NC$

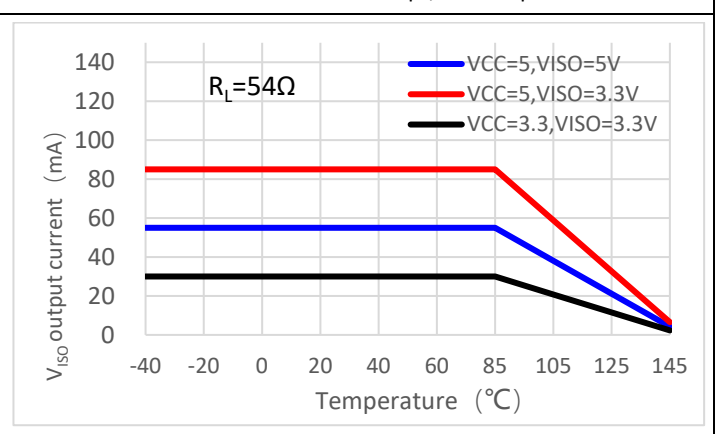
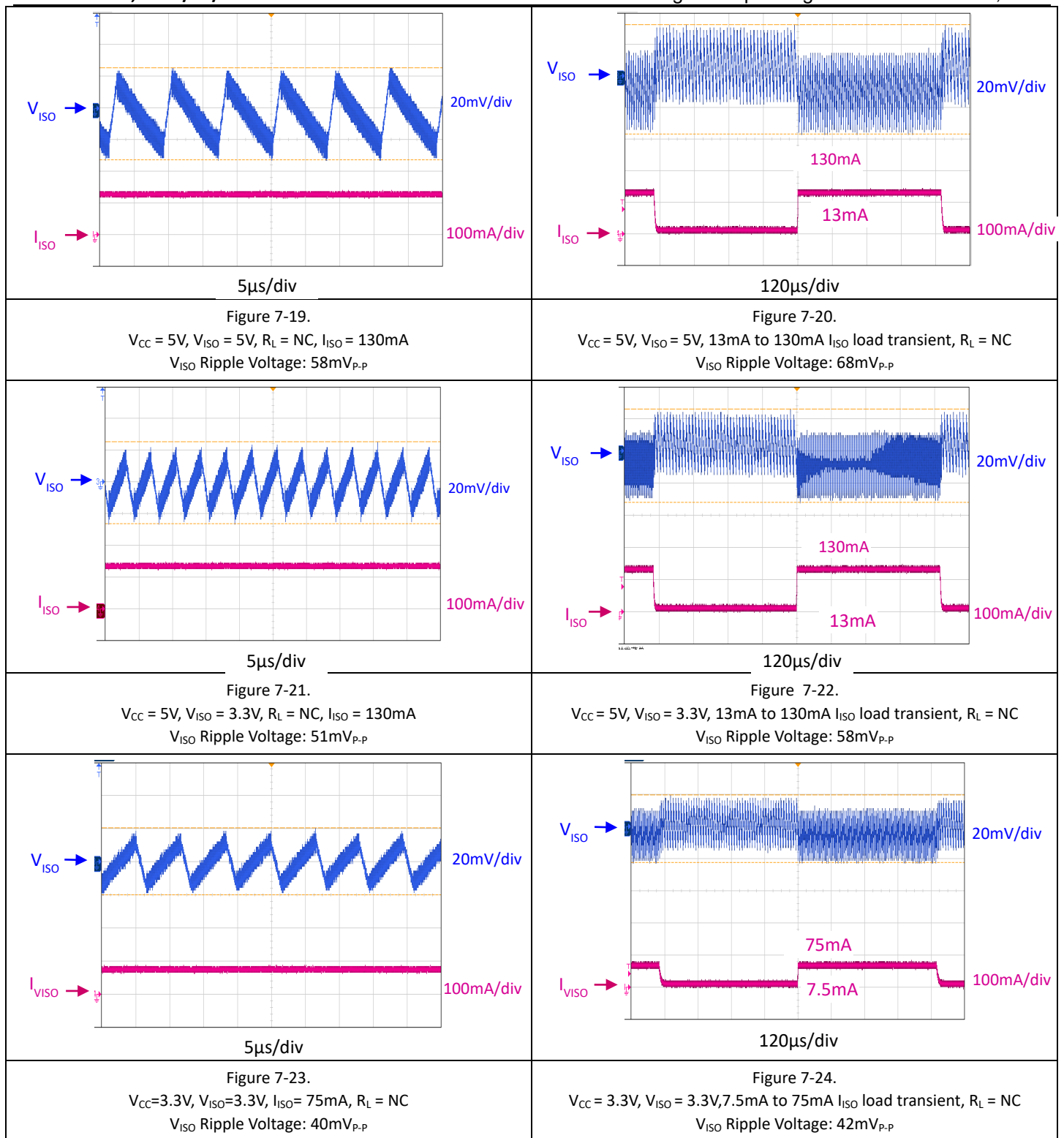


Figure 7-18.
Maximum output current from V_{ISO} vs. temperature with $R_L = 54\Omega$
CA-IS3092x: DR = 500kbps, $C_L = 2nF$
CA-IS3098x: DR = 20Mbps, $C_L = 200pF$



8. Parameter Measurement Information

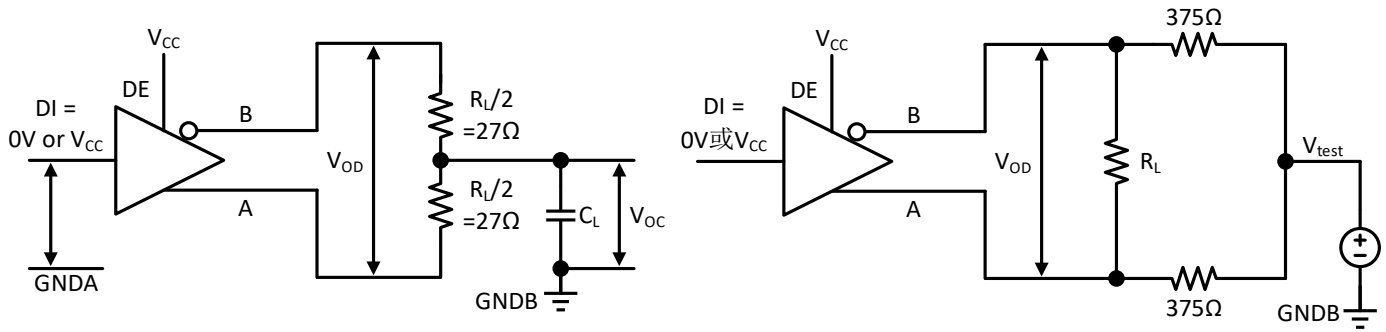


Figure 8-1. Driver DC Test Circuit

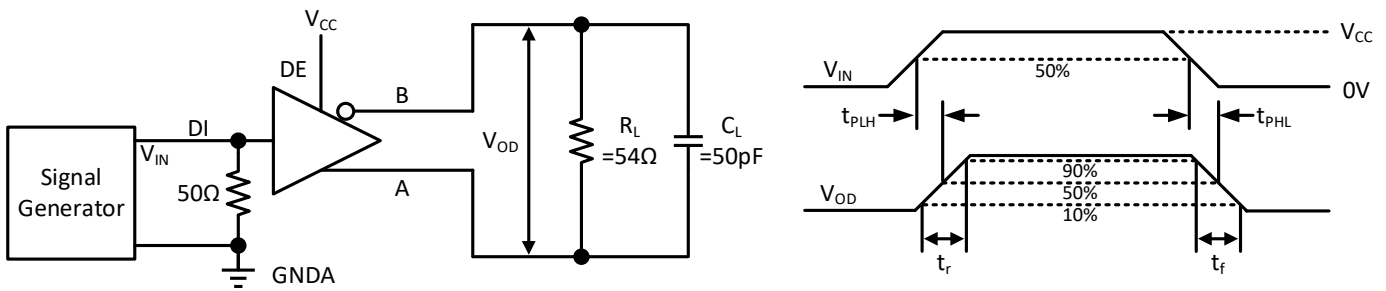


Figure 8-2. Driver Propagation Delays

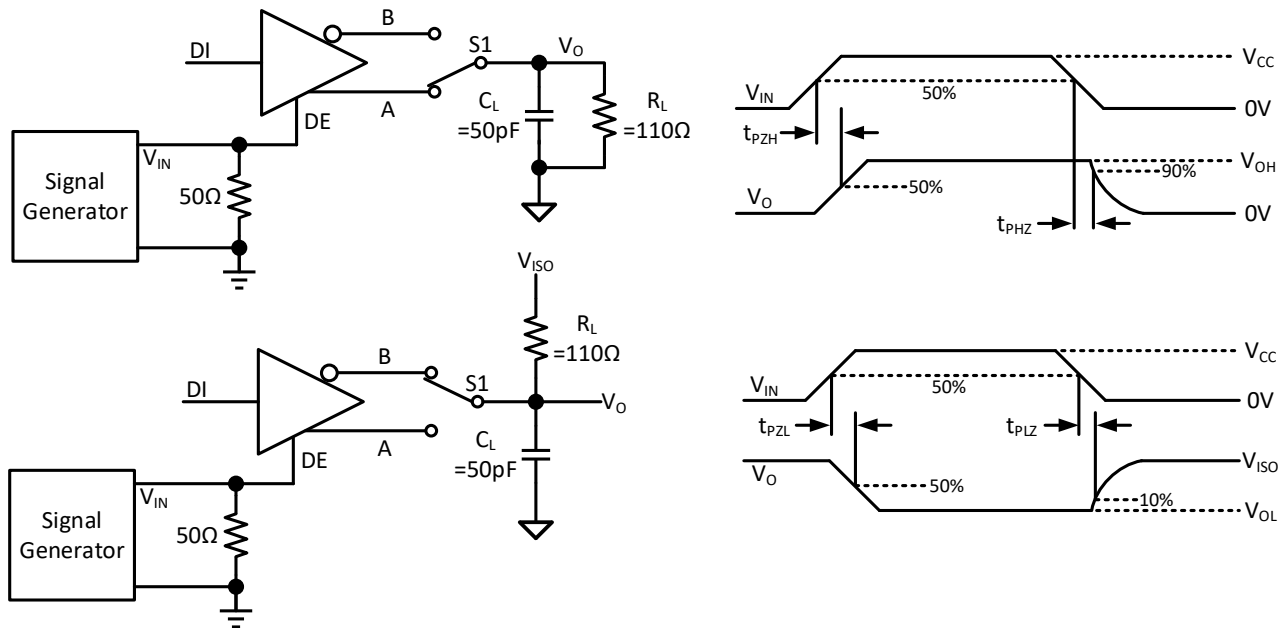


Figure 8-3. Driver Enable and Disable Times

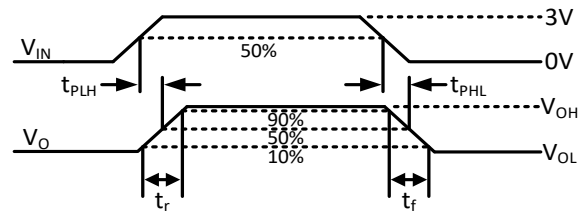
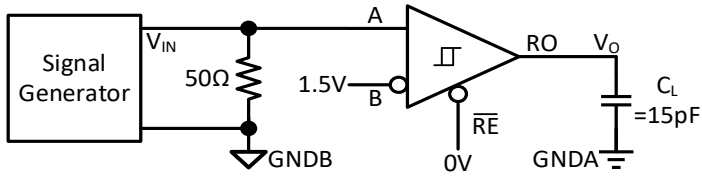


Figure 8-4. Receiver Propagation Delays

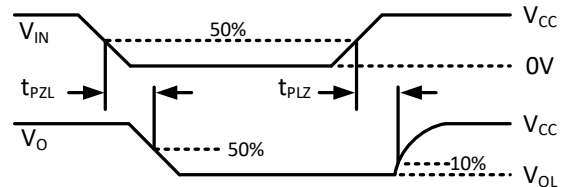
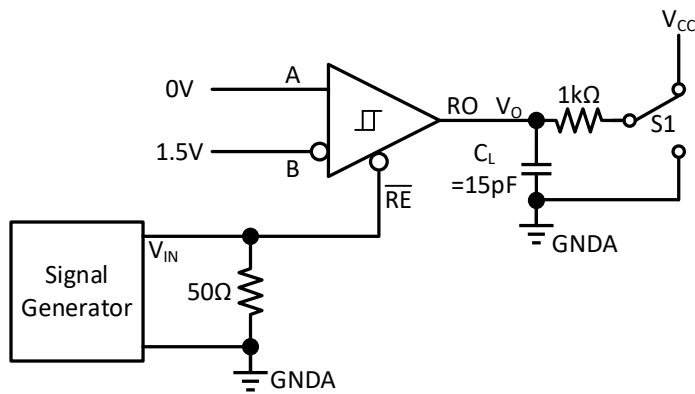
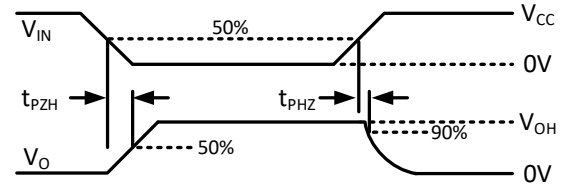
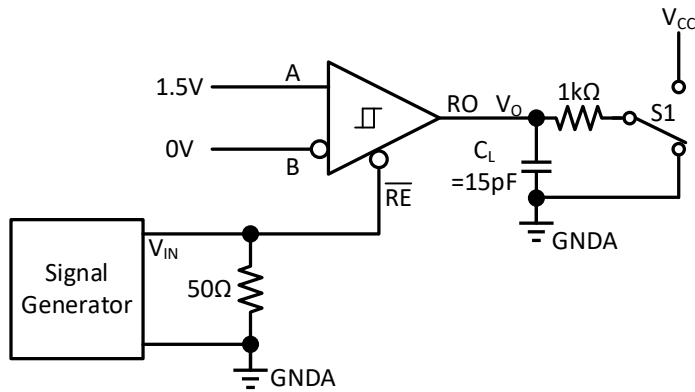


Figure 8-5. Receiver Enable and Disable Times

Notes:

1. $R_L = 54 \Omega$ for RS-485
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

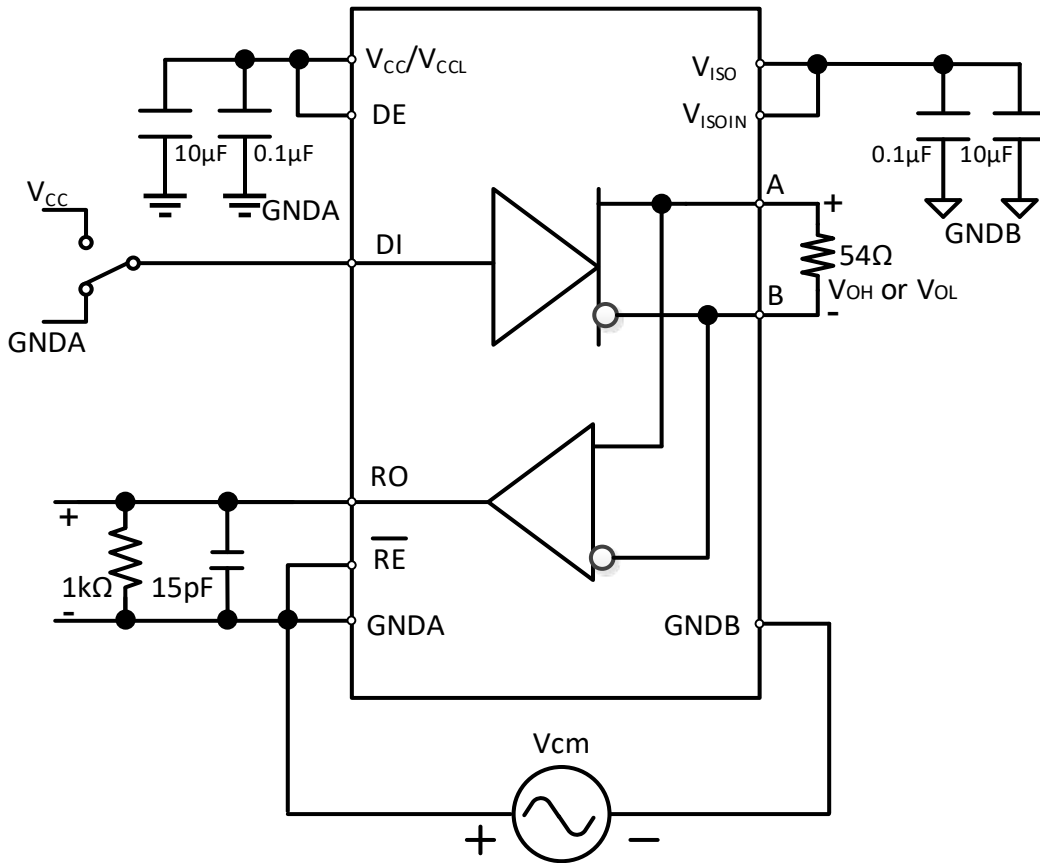


Figure 8-6. Common Mode Transient Immunity (CMTI) Test for the Half-duplex

9. Detailed Description

The CA-IS3092/CA-IS3098 isolated half-duplex RS-485 transceivers provide up to $5kV_{RMS}$ of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to $150kV/\mu s$ common mode transient immunity, allow up to 20Mbps (CA-IS3098) or 0.5Mbps (CA-IS3092) communication across an isolation barrier. Power isolation is achieved with an integrated DC-DC converter to generate a regulated 3.3V or 5V supply for the cable-side circuit. These devices do not require any external components other than bypass capacitors and bus termination resistors to realize an isolated RS-485 port. Robust isolation coupled with extended ESD protection and increased speed enables efficient communication in noisy environments, making them ideal for long distance transmission and multi-drop communication in a wide range of applications such as motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs etc. systems. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state.

9.1. Logic Input

The CA-IS309x devices include three logic inputs on the logic side: receiver enable, driver enable and driver digital input. The driver enable control DE pin has an internal weak pull-down to GND, while the digital input DI and receiver enable pins have an internal pull-up to V_{CC}/V_{CCL} , see Figure 9-1 the input equivalent circuit.

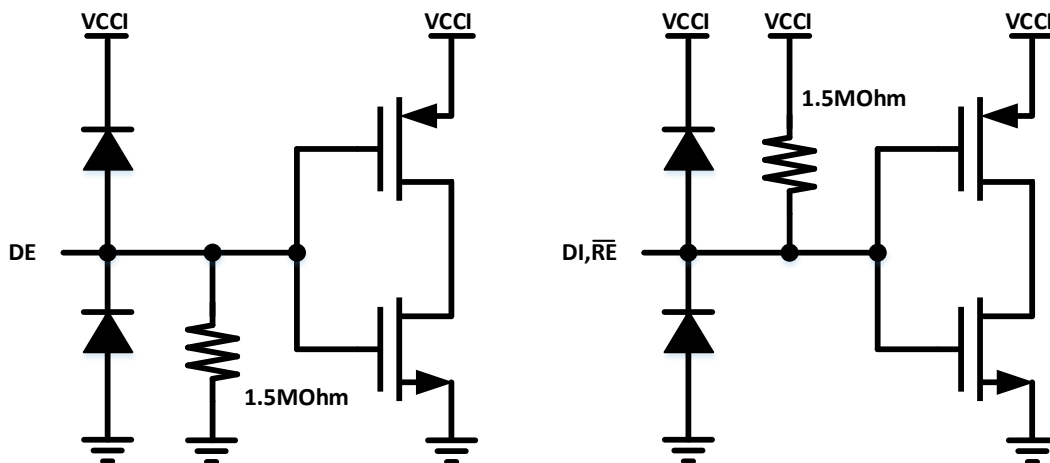


Figure 9-1. Input equivalent circuit

9.2. Fail-Safe Receiver

The receiver reads the differential input from the bus line (A and B) and transfers this data as a single-ended, logic-level output RO to the controller. Driving the enable input \overline{RE} low to enable the receiver. Driving \overline{RE} logic high to disable the receiver. RO is high impedance when \overline{RE} is logic high. The \overline{RE} pin has an internal pull-up resistor to V_{CC} for CA-IS3092W/CA-IS3098W or V_{CCL} for CA-IS3092VW/CA-IS3098VW.

The CA-IS309x family of RS-485 transceivers do not require external fail-safe bias resistors because a true fail-safe feature is integrated into the devices. In true fail-safe, the receiver's positive-going input threshold is $V_{IT+(IN)}$ ($-110mV$, typ. and $-50mV$, max.), if the differential receiver input voltage of $V_A - V_B$ is greater than or equal to $V_{IT+(IN)}$, RO is logic high when \overline{RE} is low; RO is logic low when $V_A - V_B$ is less than or equal to $V_{IT-(IN)}$ in case the receiver is enabled; thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, see Table 9-1 the receiver truth table. Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1. Receiver Truth Table

DIFFERENTIAL INPUT: $V_{ID} = (V_A - V_B)$	ENABLE (\overline{RE})	OUTPUT (RO)
$V_{IT+(IN)} \leq V_{ID}$	L	H
$V_{IT-(IN)} < V_{ID} < V_{IT+(IN)}$	L	Indeterminate
$V_{ID} \leq V_{IT-(IN)}$	L	L
X	H	Hi-Z
Open/Short/Idle	L	H
X	Open	Hi-Z

Notes:

- X = don't care; H = high level; L = low level; Hi-Z = high impedance.
- \overline{RE} has an internal weak pull-up to V_{CC} .

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs on the bus lines A and B. The truth table for the transmitter is provided in Table 9-2, the driver enable control DE pin has an internal weak pull-down to GNDA, see Figure 9-1 the input equivalent circuit; while the digital input DI pin has an internal pull-up to V_{CC} for CA-IS3092W/CA-IS3098W or V_{CCL} for CA-IS3092VW/CA-IS3098VW. The driver outputs and receiver inputs on the bus side are protected from $\pm 20kV$ electrostatic discharge (ESD) to GNDB, as specified by the Human Body Model (HBM). The driver outputs also feature short-circuit protection and thermal shutdown.

Table 9-2. Transmitter Truth Table

T_x INPUT (DI)	ENABLE INPUT (DE)	OUTPUT	
		A	B
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z
X	OPEN	Hi-Z	Hi-Z
OPEN	H	H	L

Notes:

- X = don't care; H = high level; L = low level; Hi-Z = high impedance.
- DE pin has an internal weak pull-down to GNDA, and DI pin has an internal pull-up to V_{CC}/V_{CCL} .

9.4. Protection Functions

9.4.1. Signal Isolation and Power Isolation

The CA-IS309x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. Also, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side.

9.4.2. Undervoltage Lockout

Both CA-IS3092 and CA-IS3098 devices have undervoltage detection on V_{CC} supply terminal, the CA-IS3092VW/CA-IS3098VW also feature undervoltage detection on V_{CCL} supply terminal, that place the device in protected mode during an undervoltage event on V_{CCL} or/and V_{CC} , see Table 9-3 and Table 9-4. Once the undervoltage condition is cleared and the supply voltage has returned to a valid level, the devices transition to normal mode. The host controller should not attempt to send or receive messages until the device enters normal operation.

Table 9-3. CA-IS3092W/CA-IS3098W Undervoltage Lockout

V _{CC}	DEVICE STATE	BUS OUTPUT	RXD
> V _{CC(UVLO+)}	Normal	Per TXD	Mirrors Bus
< V _{CC(UVLO-)}	Protected mode	High Impedance	High Impedance

Table 9-4. CA-IS3092VW/CA-IS3098VW Undervoltage Lockout

V _{CC}	V _{CCL}	DEVICE STATE	BUS OUTPUT	RXD
> V _{CC(UVLO+)}	> V _{CCL(UVLO+)}	Normal	Per TXD	Mirrors Bus
< V _{CC(UVLO-)}	> V _{CCL(UVLO+)}	Protected mode	High Impedance	High Impedance
> V _{CC(UVLO+)}	< V _{CCL(UVLO-)}	Protected mode	High Impedance	High Impedance
< V _{CC(UVLO-)}	< V _{CCL(UVLO-)}	Protected mode	High Impedance	High Impedance

9.4.3. Thermal Shutdown

If the junction temperature of the CA-IS309x device exceeds the thermal shutdown threshold T_{J(shutdown)} (180°C, typ.), the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device(160°C, typ.).

9.4.4. Current-Limit

The CA-IS309x protect the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to 12V by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit fault. The transmitter returns to normal operation once the short is removed.

9.5. Isolated Supply Output

The integrated DC-DC converter provide up to 650mW of isolated power with +3.3V or +5V fixed output voltage configurations. , depending on the SEL pin status, see Table 9-5 for the supply configurations of CA-IS309x devices. Get the SEL pin fixed (connect to V_{ISO} or GNDB) before power on the transceivers.

Table 9-5. Supply Configuration

SEL INPUT	V _{CC}	V _{ISO}
Shorted to V _{ISO}	5 V	5V
Shorted to GNDB or floating	5 V	3.3V
Shorted to GNDB or floating	3.3 V ¹	3.3V ²

Notes:

1. V_{DD} = 3.3 V, SEL shorted to V_{ISO} (essentially V_{ISO} = 5 V) is not recommended.
2. The SEL pin has a weak pull-down internally. However, for V_{ISO} = 3.3 V, the SEL pin should be connected to the GNDB externally, especially in the noisy system.

The maximum output current from V_{ISO} is shown as Table 9-6. Note that the I_{ISO} value in Table 9-6 is the maximum output current at +25°C with data rate x load capacitance < 0.5Mbps x 2nF for CA-IS3092W/CA-IS3092VW (20Mbps x 200pF for CA-IS3098W/CA-IS3098VW). As the increase of temperature, especially when the temperature exceeds +85°C, the maximum load current will be decreased, see more details in Figure 7-14, Figure 7-16, and Figure 7-18.

Table 9-6. Maximum Output Current of V_{ISO} @ $T_A = 25^\circ C$

Supply voltage V_{CC} (V)	V_{ISO} (V)	R_L (Ω) between CANH and CANL	I_{ISO} (mA)
4.5~5.5	5	NC ¹	130
4.5~5.5	3.3		130
3.15~3.6	3.3		75
4.5~5.5	5	100	80
4.5~5.5	3.3		105
3.15~3.6	3.3		40
4.5~5.5	5	54	55
4.5~5.5	3.3		85
3.15~3.6	3.3		30

Note:

1. NC means no-load connection between CANH and CANL.

10. Applications Information

10.1. Overview

The CA-IS3092/CA-IS3098 family of half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Because of high peak currents flowing through V_{CC} and V_{ISO} supplies, bulk capacitance of typical $10\mu F$ (or at least $4.7\mu F$) is recommended on both pins. Higher values of bulk capacitors are helpful to reduce noise and ripple further and enhance performance, see Figure 10-1 the typical application circuit. Make sure there is no data transmission during the CA-IS309X power up.

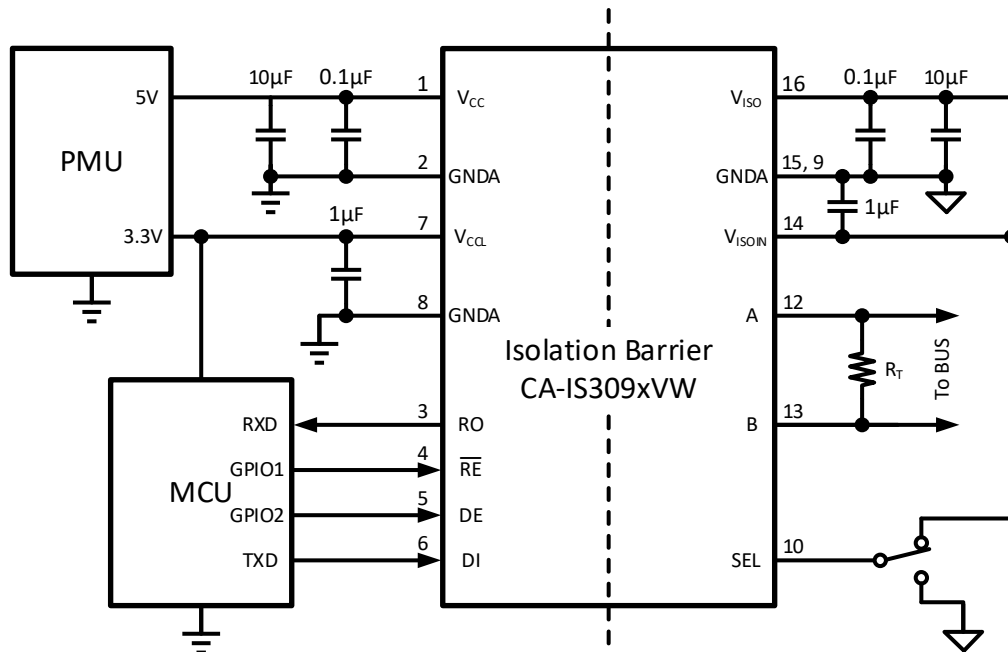


Figure 10-1. Typical application circuit

10.2. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, Figure 10-2. The maximum recommended data rate in the RS-485 network is 10Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original RS-485 standard, new RS-485 transceivers and cables are pushing the limit of RS-485 far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance(Z_0) of the cable, and keep stub lengths off the main line as short as possible. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

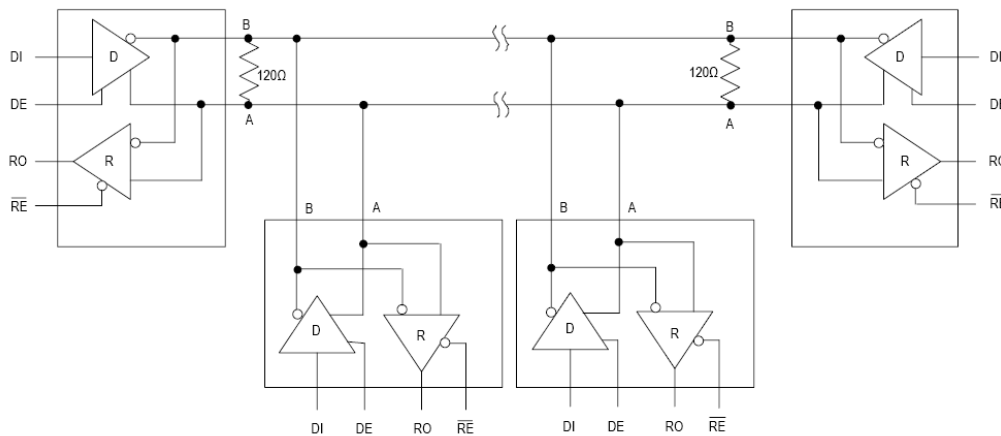


Figure 10-2. Typical isolated half-duplex RS-485 application circuit

10.3. 256 transceivers on the bus

The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32 (375Ω). The CA-IS309x transceivers have a 1/8-unit load (96kΩ) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line.

10.4. PCB Layout

Careful PCB layout is critical to achieve clean and stable communication operation. It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the minimum 0.1μF//10μF decoupling capacitors between V_{CC} and GNDA, between V_{ISO} and GNDB are recommended. For the individual logic supply input V_{CCL} and V_{ISOIN} , we recommend to use a 1μF ceramic capacitors with X5R or X7R between V_{CCL} pin and GNDA, V_{ISOIN} and GNDB. Place the bypass capacitors, and the CA-IS309x IC on the same PCB layer. Place decoupling capacitors as close as possible to the CA-IS309x device pins, see Figure 10-3 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths.

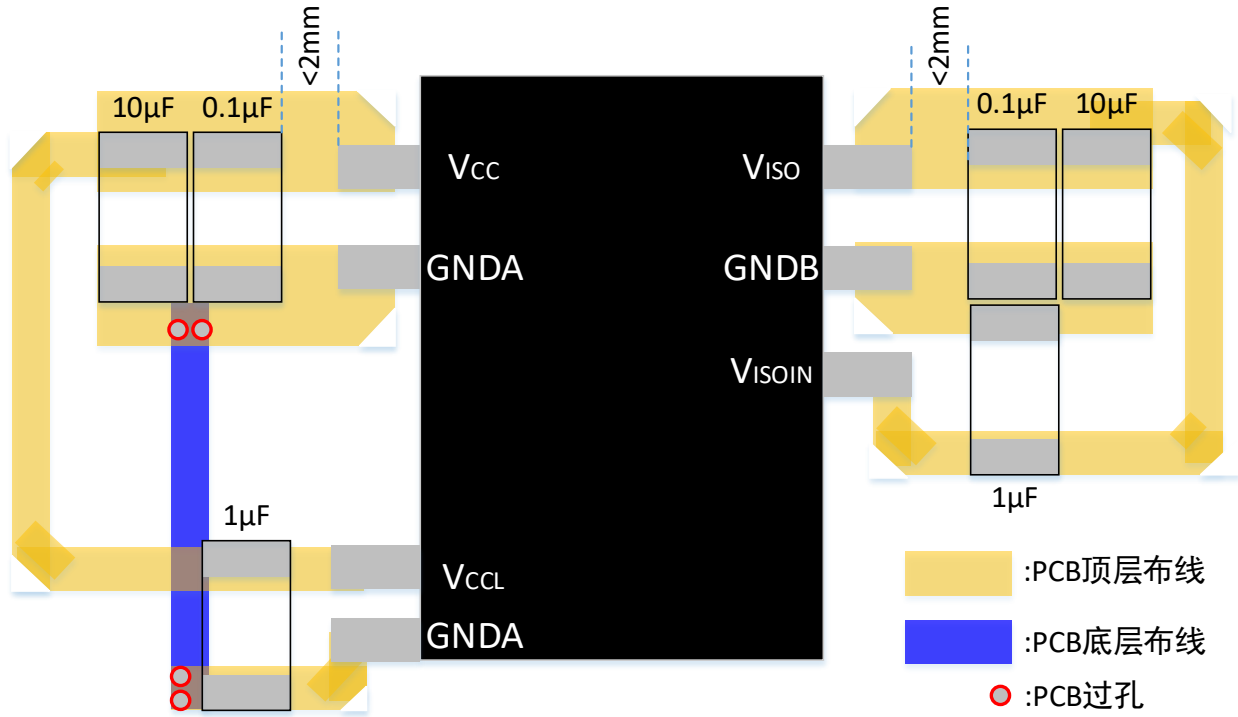
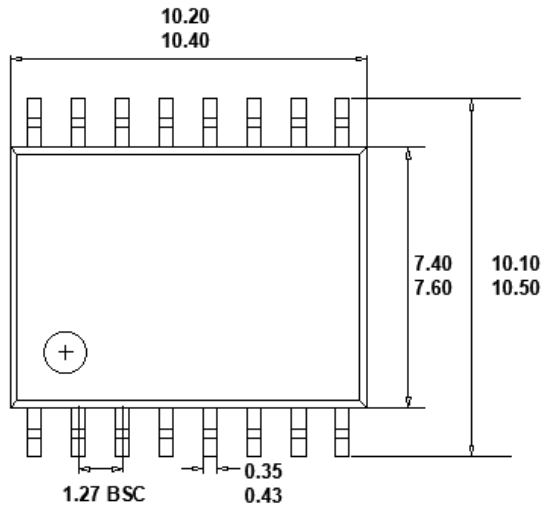


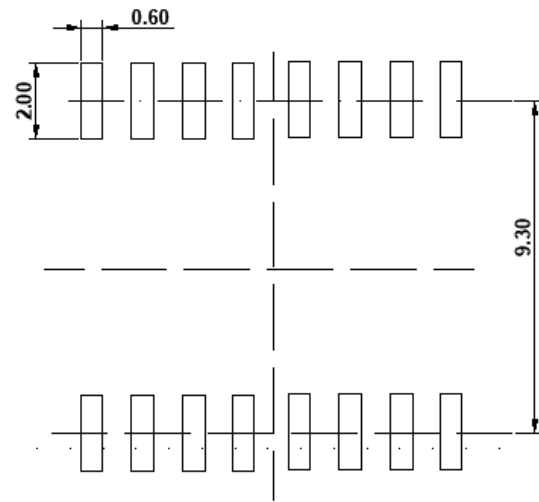
Figure 10-3. Recommended PCB Layout

11. Package Information

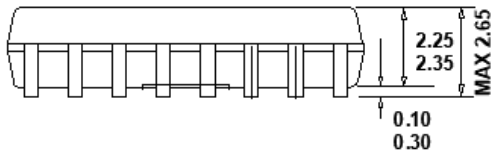
16-Pin Wide Body SOIC Package Outline



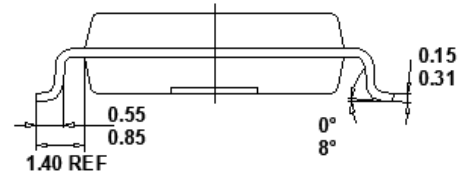
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

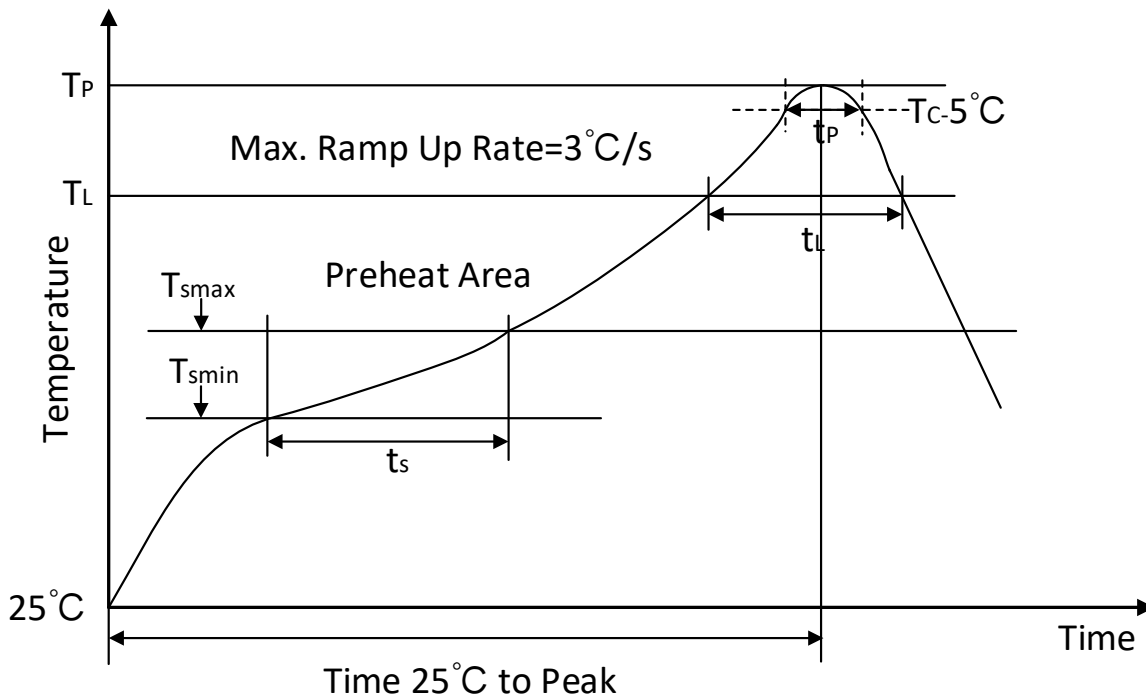
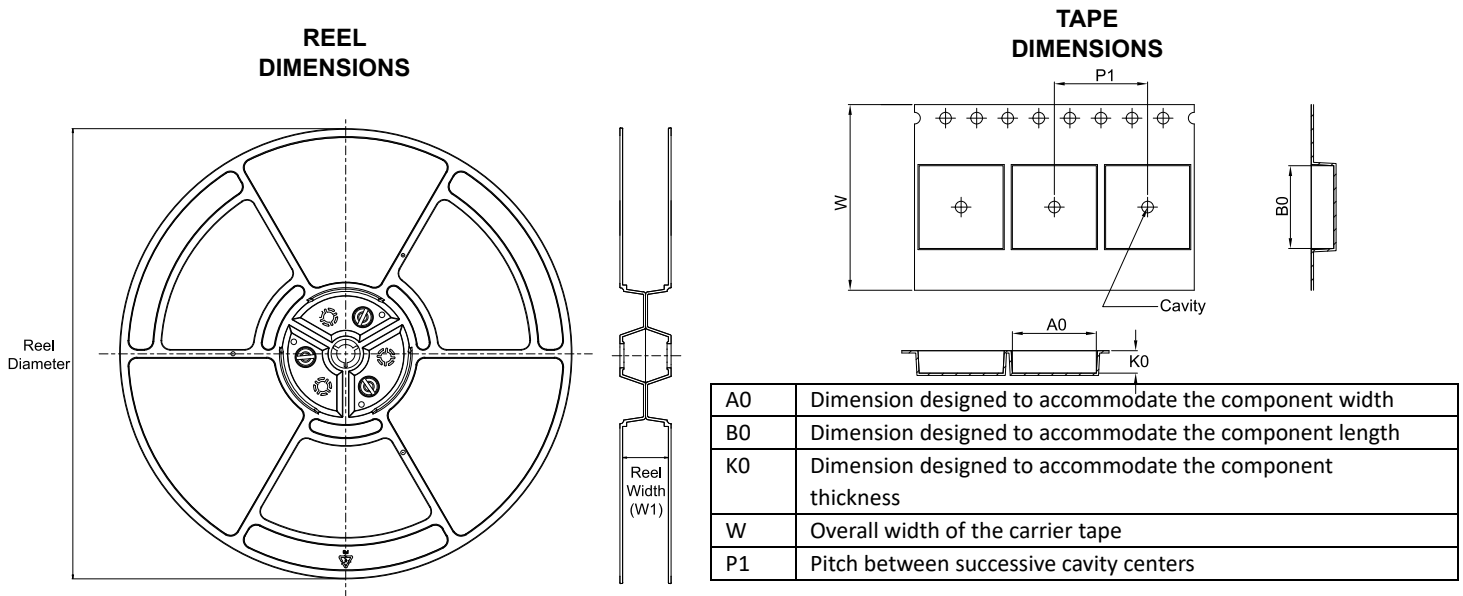
12. Soldering Temperature (reflow) Profile


Figure. 12-1 Soldering Temperature (reflow) Profile

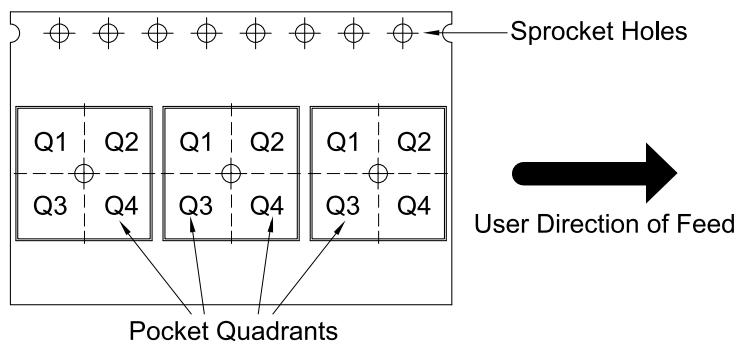
Table. 12-1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 °C to Peak)	3°C /second max
Time of Preheat temp(from 150 °C to 200 °C)	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25°C to peak temp	8 minutes max

13. Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3092W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3092VW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3098W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3098VW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

14. Important Statement

The above information is for reference only and intended to help Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.



<http://www.chipanalog.com>